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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,205	04/21/2004	Henry A. Bonges III	FIS920040088US1	3204

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

M'A

Office Action Summary	Application No.	Applicant(s)
	10/709,205	BONGES ET AL.
	Examiner	Art Unit
	Helen Rossoshek	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16 and 17* is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *14,15 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/709,205 filed 04/21/2004.

2. Claims 1-20 are pending in the Application.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

4. Claims 2-15 and 18-20 are objected to because of the following informalities: there is insufficient antecedent basis for these claims. First "A method" has to replaced by –The method--

claim 4 line 2 after "of" insert space

claim 4 and 20 have insufficient antecedent basis: it is not clear if "a cell" is one of the aforementioned (in claims 2 and 18 respectively)"cells in a byte array"

claim 11 line 6 after "fifth" insert –code--

claims 14 and 15 are objected to because of using capitals letters for term "UNREACHABLE" in claim 14. Examiner suggests to uniform representation of this term in the claims, since it appears in others claims not in capital letters.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhat et al. ("Special Purpose Architecture for Accelerating Bitmap DRC", 25-29 June 1989, Design Automation, 26th Conference on, Pages:674 – 677) in view of Bell (US Patent 6,615,393).

With respect to claim 1 Bhat et al. teaches a method of performing latch up check on an integrated circuit (IC) design (within performing design rule check specifically for width and space checking on design integrated circuit) (abstract, Page 674) comprising the steps of: computing a combined least enclosing rectangle enclosing a conductor region shape and contact shapes (by determining rectangular geometries in the layout of the design IC) (Page 674, left column); rasterizing the conductor region shape and the contact shapes (using rasterized layout as a bitmap pattern, such as pixel array) (Page 674, left column); iteratively expanding the contact shapes within the conductor region shape using a cellular algorithm (within a window flexible in size using a concept of shrink/expand instructions iteratively processing rectangular geometries using cellular algorithm as manipulating with grid of cells (pixels) in subsections or windows (contact shapes) with very small instruction set) (Page 674, left, right columns); generating shapes representing an unreachable area of the conductor region shape (using algorithm for design rule check (DRC) for generating the check layer for checking rule violations in four directions – horizontal (left to

right), vertical (top to bottom), along the 45° direction (top to bottom) and along the 135° direction (top to bottom) including spacing checks based on bitmap layout (Page 675, left column); and checking the shapes representing the unreachable area of the conductor region shape against junction shapes in the design (within generating check layer and performing layout analysis for determining space rule violation as shown on the Fig. 3.1 representing check layer) (Page 675, left column), and reporting to a designer any junction shapes which intersect the unreachable area as errors within generating the error layer as shown on the Fig. 3.2 containing error positions corresponding to the direction in which checking was performed showing 1's for error and 0's for no error (Page 675, left and right columns). However Bhat et al. lacks specifics regarding spacing rules, such as unreachable area as error. Bell teaches the verification process of the semiconductor fabrication process using the concept of determination of the maximum spacing within a layer as electrical distance during latchup checking to determine the maximum distance to determine the boundary of unreachable area (col. 1, ll.60-67; col. 2, ll.1-2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Bell to teach the specifics subject matter Bhat et al. does not teach, because it provides a method and apparatus for bounding sizing of shapes that can efficiently determine sizing of shapes for verification of the integrated circuit design including electrical distance (unreachable area) check quickly and accurately (col. 2, ll.30-35).

With respect to claims 2-13 Bhat et al. teaches:

Claim 2: including the steps of: representing the contact shapes as cells in a byte array (as shown on the Fig. 2.1 depicting a bitmap representation of a single layer in the layout polygons as a array of pixels) (Page 674, right column); and exploring the conductor region shape by expanding the conductor region shape into neighboring cells of the byte array (within window processor architecture for implementation of rasterized layout shown on the Fig. 2.1 using shrink/expand instructions to perform DRC design IC) (Page 674, left column);

Claim 3: further including the step of periodically skipping expanding corner cells of the contact shapes (within processing pixels up to 4 times while the other only ones) (Page 674, right column);

Claim 4: further including the step of restricting the number of directions in which a cell can expand (associating the number of directions for expanding with the number of directions of checking cells on the check layer) (Page 675, left column);

Claim 5: further including the step of creating a 2-dimensional byte array of sufficient size to rasterize the enclosing rectangle at a resolution of "l" (within the widow processor across the entire layout checking if the bitmap pattern within the window is valid, and each pixel of the bitmap is processed n^2 for a window of size n x n) (Page 674, left column), wherein the width and height of each cell in the array corresponds to the value "l" (within each pixel as elementary square having length and width = λ, where λ is the unit in which the design rules are expressed) (Page 674, right column);

Claim 6: including the step of initializing each cell of the byte array to a first code representing an empty cell (within white pixels (empty) if it does not describe any layout polygon) (Page 674, right column);

Claim 7: further including the step of converting the least enclosing rectangle to raster format in the byte array by inserting a second code into each cell intersected by an edge of the rectangle shape (within black pixels which form a part of region within any layout poilygon) (Page 674, right column);

Claim 8: further comprising the step of converting the conductor region shape to raster format in the byte array by inserting a third code into each cell intersected by an edge of the conductor region shape (within edge pixels, which are black pixels and form the polygon boundary) (Page 674, right column);

Claim 9: further comprising the steps of: converting the contact shapes to raster format in the byte array by inserting a fourth code into each cell intersected by an edge of a contact shape (within generating a concave corner pixels showing two edges forming a part of a layout polygon boundary and convex corner pixels showing no edges forming a part of a polygon boundary) (Page 674, right column; Page 675, right column); and recording the address of each of these cells in a frontier list (within a cell shown on the Fig. 4.1, which is one of components of the processing elements construing design rule checker chip, wherein cell contain a register for storing bitmap data of each pixel including neighbor information) (Page 676, left column);

Claim 10: further comprising the step of establishing a maximum distance to be searched (within limited of the length of the maximum rule that can be checked, and is 4 λ) (Page 675, right column; Page 676, right column);

Claim 11: further comprising the steps of: expanding the contact shapes by traversing the frontier list one cell at a time and examining the cell's neighbor cells as to whether they are empty or not (within shrink/expand operations, which involves checking the neighbor pixels and determining if they empty (white), making the pixel under checking is made white with the consideration of the length of the maximum rule using the register of the cells shown on the Fig. 4.1 for storing bitmap data including neighbor information for use during shrink/expand operations) (Page 675, right column; Page 676, left column); inserting a fifth into the neighbor cell and recording its location in a new frontier list if a neighbor cell is empty (within checking the neighbor pixels and determining if they empty (white), making the pixel under checking is made white) (Page 675, right column); and not expanding into it if a neighbor cell is not empty (using rule aligners to generate control signals for plane modules shown on the Fig. 4.1, necessary hardware to combine neighbor information for use shrink/expand operations) (Page 676, left column);

Claim 12: further comprising the steps of: expanding cells which are recorded in the new frontier list (within shrink/expand operations, which involves checking the neighbor pixels and determining if they empty (white), making the pixel under checking is made white with the consideration of the length of the maximum rule using the register of the cells shown on the Fig. 4.1 for storing

bitmap data including neighbor information for use during shrink/expand operations, wherein iteration is available up to 4 times) (Page 675, right column; Page 676, left column; Page 674, right column); and inserting a fifth code into the neighbor cell and recording its location in the new frontier list if a neighbor cell is empty (within checking the neighbor pixels and determining if they empty (white), making the pixel under checking is made white, wherein iteration is available up to 4 times) (Page 675, right column; Page 674, right column); and not expanding into it if a neighbor cell is not empty (using rule aligners to generate control signals for plane modules shown on the Fig. 4.1, necessary hardware to combine neighbor information for use shrink/expand operations, wherein iteration is available up to 4 times) (Page 676, left column; Page 674, right column);

Claim 13: further comprising the steps of: continuing to expand cells by traversing the new frontier list one cell at a time, and examining the cell's neighbor cells (within iteration which is available: up to 4 times) (Page 674, right column); and inserting a sixth code into the cell, and record its location in a third frontier list if a neighbor cell is empty (within 'A' register to store bitmap data of pixels after shrink/expand operations) (Page 675, left column).

Allowable Subject Matter

7. Claims 16, 17 are allowed. The prior art of record does not teach extracting unreachable areas of the conductor region shape by detecting chains of unreachable cells; converting unreachable areas into shapes, and returning these shapes as unreachable areas in the vector domain; checking the

unreachable areas against junction shapes in the design and flagging any junction shapes which intersect the unreachable areas as errors as claimed.

It has to be noted that claims 18-20 being dependent from allowed claim 17 can be allowed after required amendment to overcome aforementioned objection of claims 18-20.

8. Claims 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach extracting unreachable areas of the conductor region shape by traversing the byte array, row-by-row, detecting horizontal chans of unreachable cells, converting each chain into a rectangle by converting its corners into (X,Y) coordinate pairs representing positions in an original drawing space, and computing the union of these rectangles, and returning these shapes as the unreachable area of the conductor region as claimed.

Moreover, amendment of claim 14 is required to overcome aforementioned objection of the claims 14 and 15.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax

phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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